1. Features

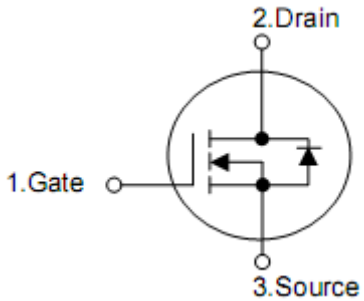
- Proprietary New Planar Technology
- $R_{DS(ON)}$=70mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

2. Applications

- DC-DC Converters
- DC-AC Inverters for UPS
- SMPS and Motor controls

3. Pin configuration

TO-3P



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNH3730A	TO-3P	KIA

5. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage [1]		V_{DSS}	300	V
Gate-to-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	Tc=25 ºC	I_D	50	A
	Tc=100 ºC	I_D	31	A
Pulsed Drain Current at V_{GS}=10V [2]		I_{DM}	200	A
Single Pulse Avalanche Energy		EAS	3044	mJ
Peak Diode Recovery dv/dt [3]		dv/dt	5.0	V/ns
Power Dissipation		P_D	305	W
Derating Factor above 25°C		P_D	2.5	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T_L T_{PAK}	300 260	ºC
Operating and Storage Temperature Range		T_J&T_{STG}	-55 to 150	ºC

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.41	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	ºC/W

7. Electrical characteristics

(T_J=25°C,unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	300	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=300V, V_{GS}=0V	-	-	1	uA
		V_{DS}=240V,T_J=125°C	-	-	100	uA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-to-Source ON Resistance [4]	$R_{DS(ON)}$	V_{GS}=10V, I_D=25A	-	70	88	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0	-	4.0	V
Forward Transconductance [4]	gfs	V_{DS}=15V,I_D=25A	-	18	-	S
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, f=1.0MHZ	-	5108	-	pF
Reverse Transfer Capacitance	C_{rss}		-	275	-	
Output Capacitance	C_{oss}		-	500	-	
Total Gate Charge	Q_g	V_{DD}=150V,I_D=25A, V_{GS}=0~10V	-	220	-	nC
Gate-to-Source Charge	Q_{gs}		-	16	-	
Gate-to-Drain (Miller) Charge	Q_{gd}		-	128	-	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD}=150V, I_D=25A, R_G=1.2Ω,V_{GS}=10V	-	25	-	nS
Rise Time	t_{rise}		-	50	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	100	-	
Fall Time	t_{fall}		-	35	-	
Continuous Source Current [4]	I_{SD}	Integral PN-diode in MOSFET	-	-	50	A
Pulsed Source Current [4]	I_{SM}		-	-	200	A
Forward Voltage	V_{SD}	I_S=25A, V_{GS}=0V	-	-	1.5	V
Reverse recovery time	t_{rr}	V_{GS}=0V ,I_F=25A, diF/dt=100A/μs	-	516	-	ns
Reverse recovery charge	Q_{rr}		-	4.16	-	uC

Note:
1) T_J=+25°C to +150°C
2) Repetitive rating; pulse width limited by maximum junction temperature.
3) I_{SD}=20A, di/dt<100 A/μs, V_{DD}<BV_{DSS}, T_J=+150°C.
4) Pulse width≤380μs; duty cycle≤2%.

8. Test circuits and waveforms

Figure 1a Safe Operating Area

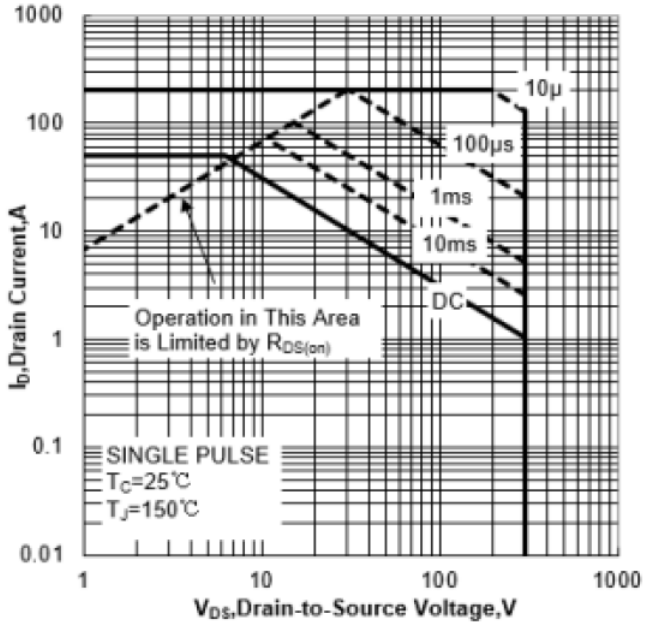


Figure 2 Power Dissipation

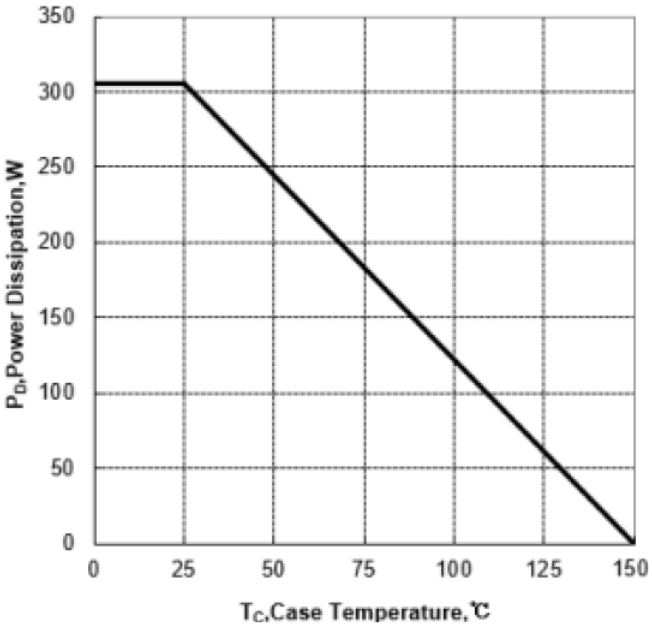


Figure 3 Max Thermal Impendance

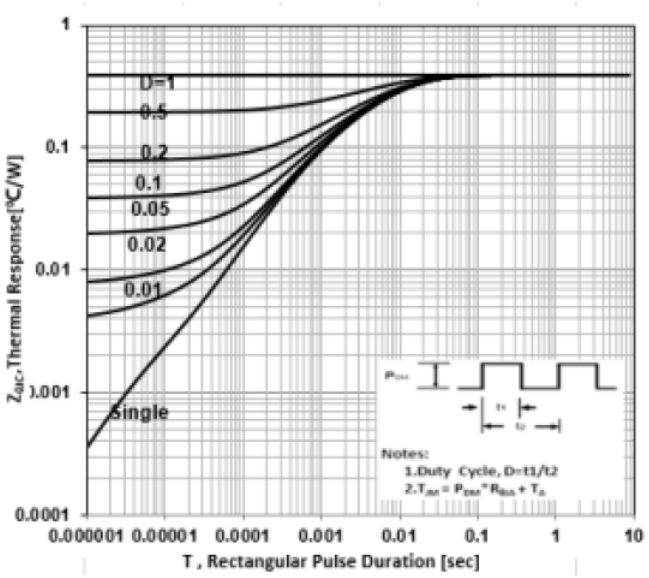


Figure 4 Typical Output Characteristics

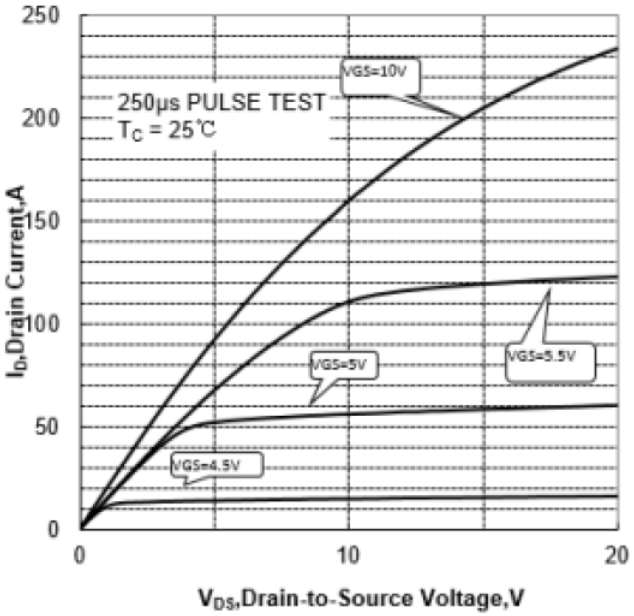


Figure 5 Typical Transfer Characteristics

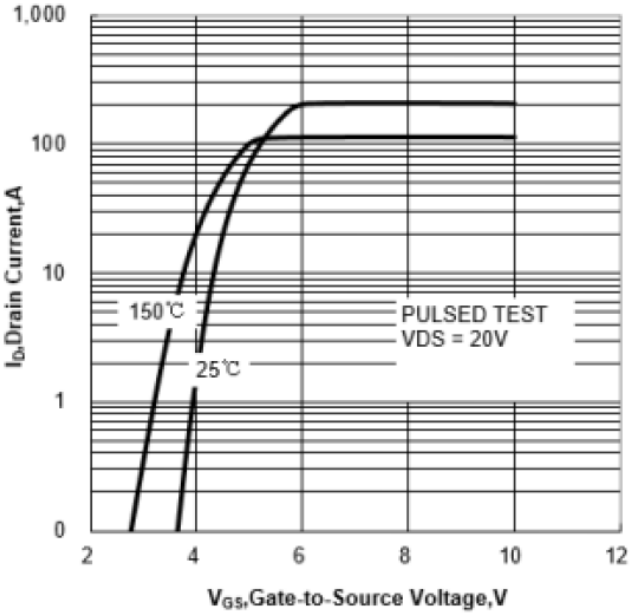


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

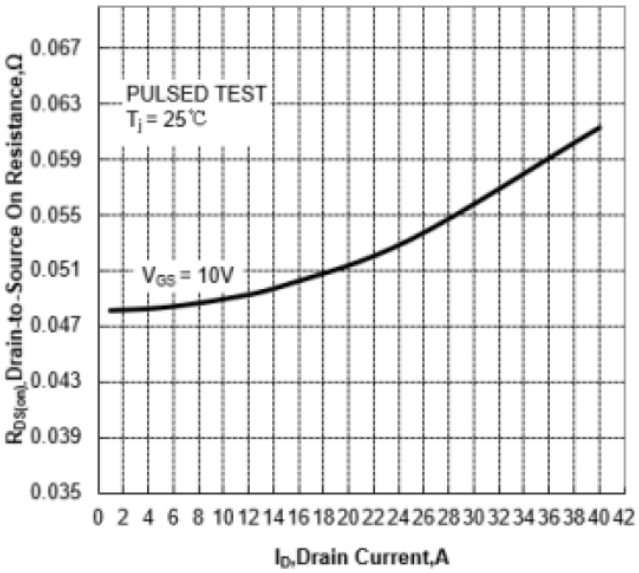


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

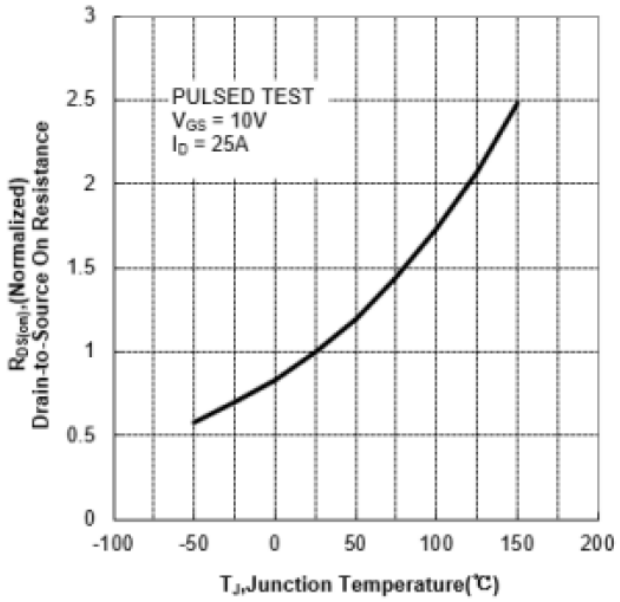


Figure 8 Typical Theshold Voltage vs Junction Temperature

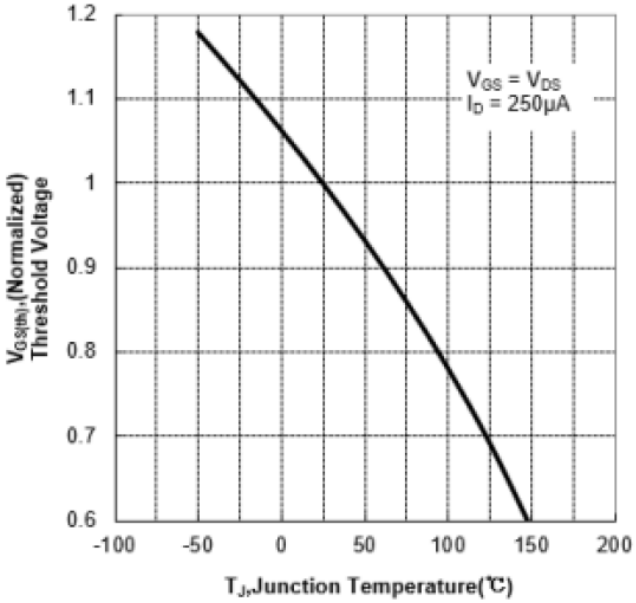


Figure 9 Typical Breakdown Voltage vs Junction Temperature

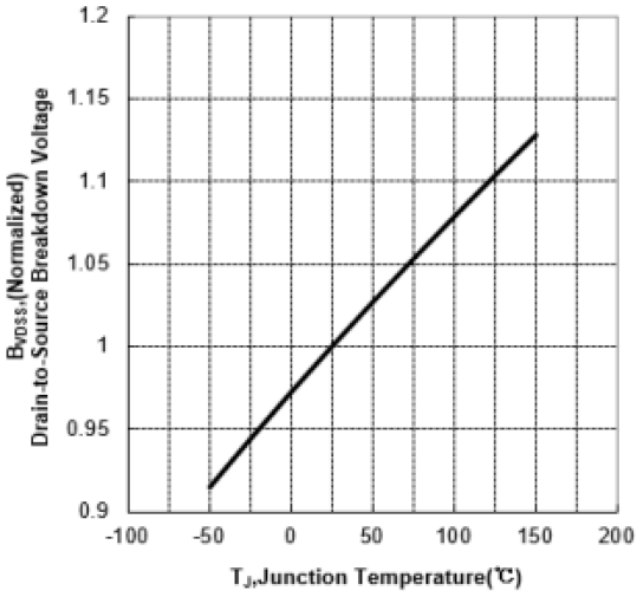


Figure 10 Typical Capacitance vs Drain to Source Voltage

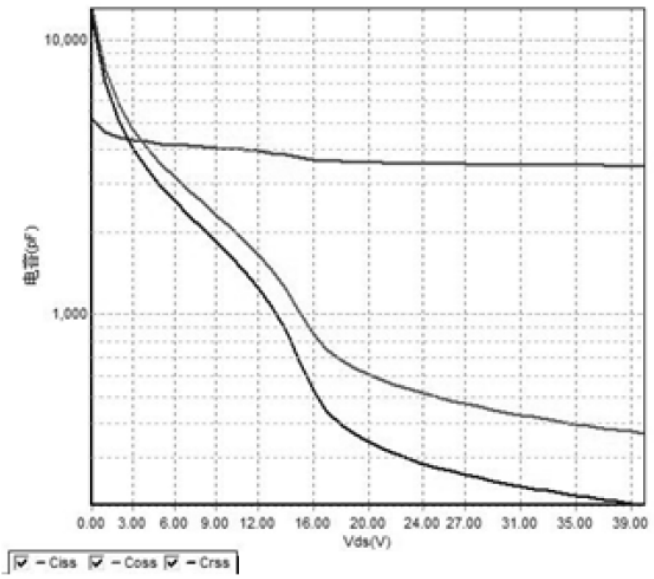
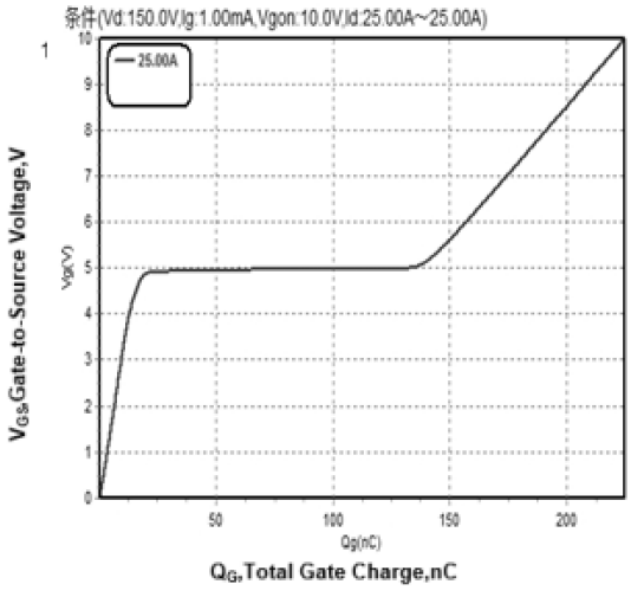


Figure 11 Typical Gate Charge vs Gate to Source Voltage



9. Test Circuits and Waveforms

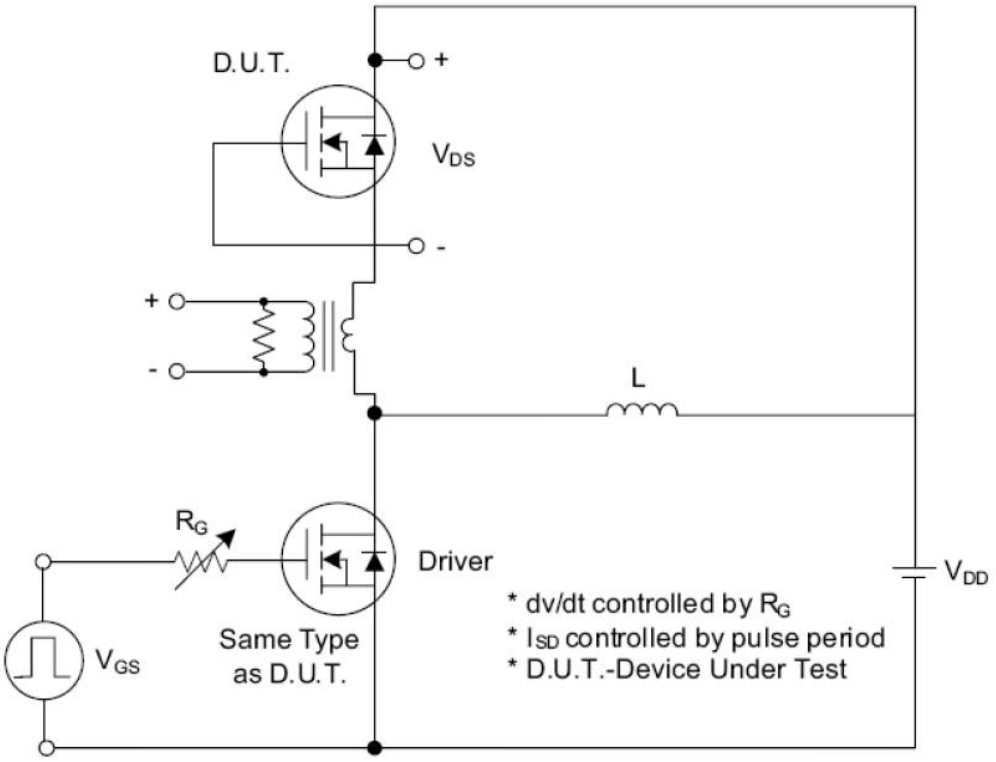


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

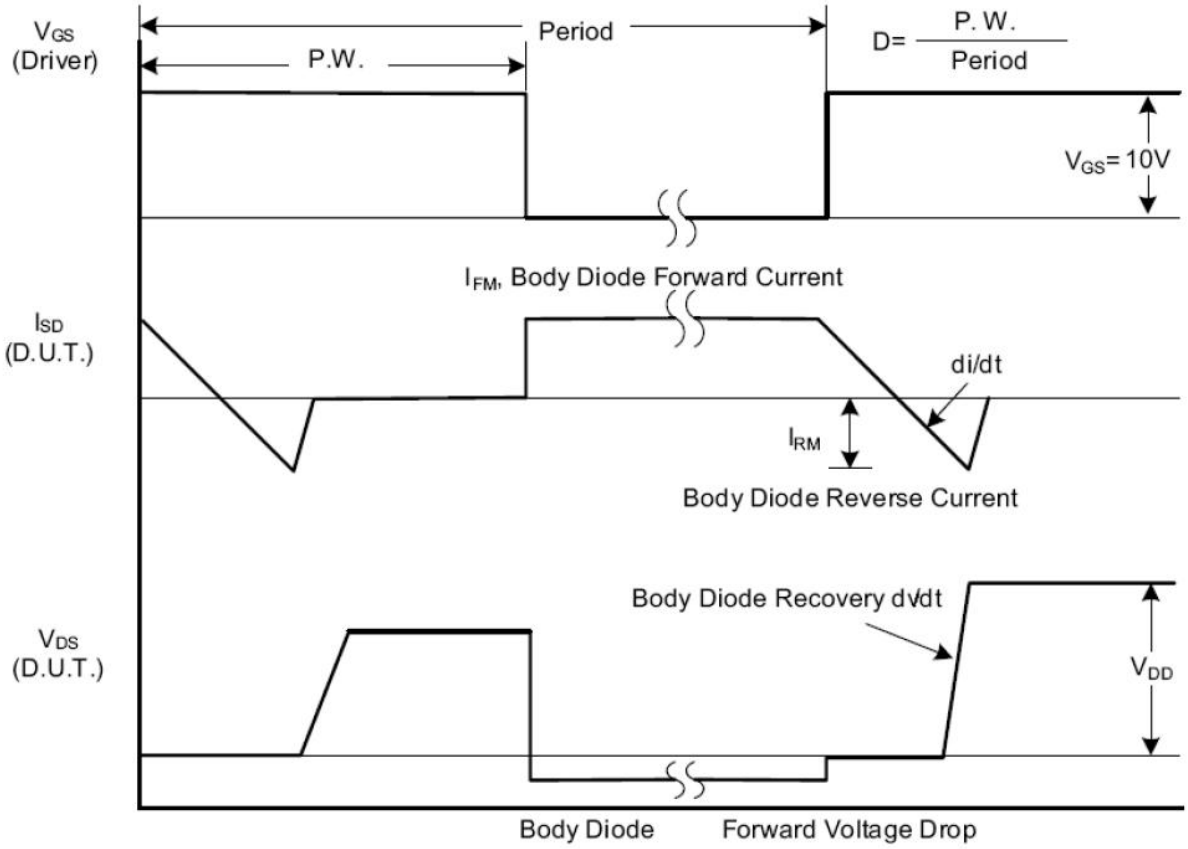


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

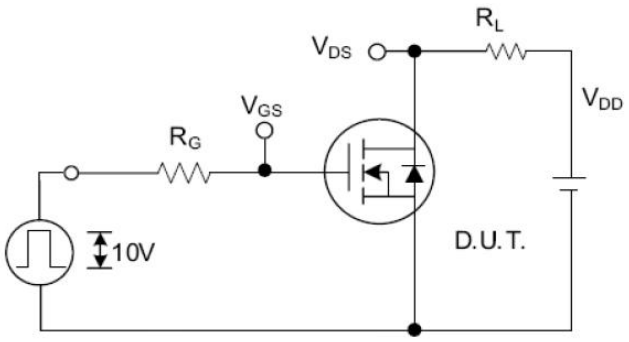


Fig. 2.1 Switching Test Circuit

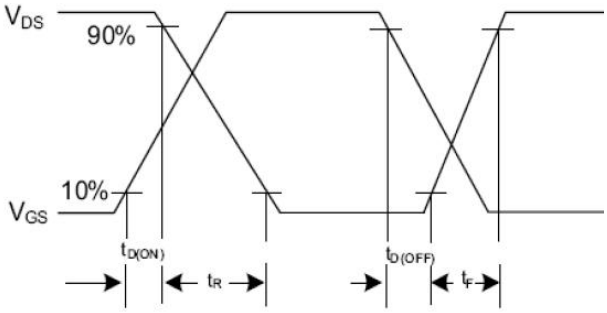


Fig. 2.2 Switching Waveforms

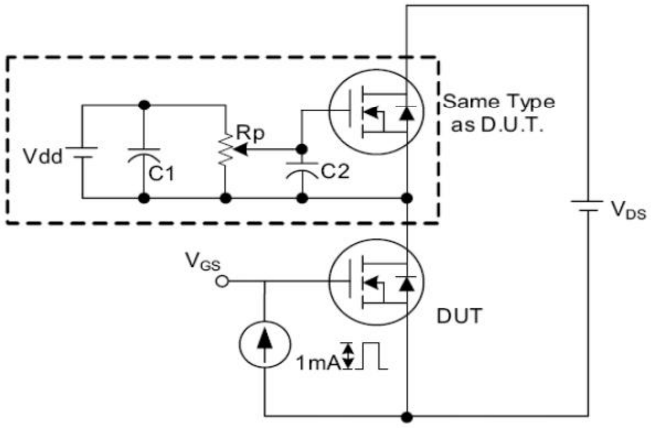


Fig. 3 . 1 Gate Charge Test Circuit

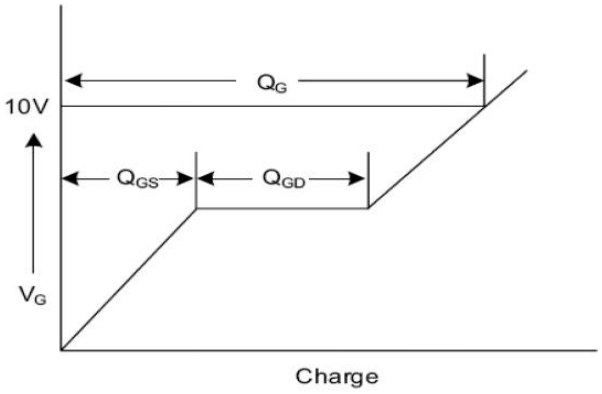


Fig. 3 . 2 Gate Charge Waveform

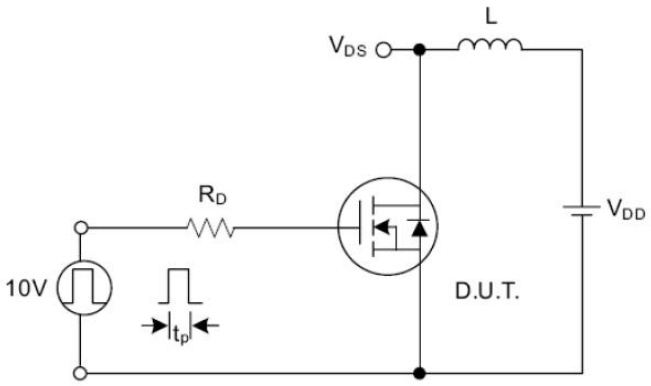


Fig. 4.1 Unclamped Inductive Switching Test Circuit

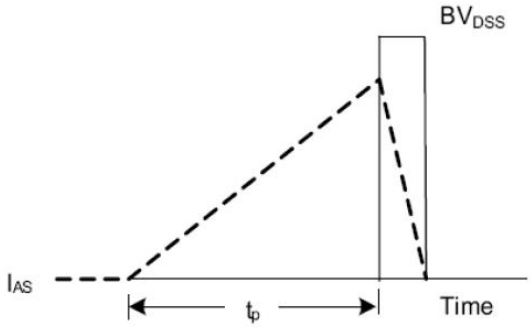


Fig. 4.2 Unclamped Inductive Switching Waveforms